APPENDIX B

PATENT

METHOD FOR PLANARIZING A THIN FILM

BACKGROUND OF THE INVENTION

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1. Field of the Invention.

The present invention relates to a method for chemical-mechanical polishing and, more particularly, to a method for chemical-mechanical polishing to form a thin film.

2. Description of the Related Art.

During the fabrication of many semiconductor circuits, the individual devices that make up the circuits are fabricated, in part, by forming a number of layers of material on a wafer and then selectively etching one or more of the layers of material to leave the individual devices. The result of this etch step, however, produces a severe topology with the individual devices forming high points and the etched-away portions forming low points.

FIG. 1 shows a cross-sectional diagram that illustrates a prior-art processed wafer 100 following the etch step that defines the individual devices that make up the circuits on wafer 100. As shown in FIG. 1, wafer 100 has a number of individual devices 110 and a number of etched-away portions 112. In addition, wafer 100 has a top surface 114 with high points defined by the top surfaces of the individual devices 110 and low points defined by the top surfaces of the etched-away portions 112.

One problem with a severe topology is that it is difficult to form a thin, planarized layer of polysilicon on this type of surface. A thin, planarized layer of polysilicon can be used to implement, for example, a local interconnect line. One well-known technique for forming planarized surfaces is known as chemical-mechanical polishing (CMP).

With CMP, an uneven surface is both chemically reacted and mechanically ground to bring down the surface until a substantially flat surface is formed. Conventional CMP processes, however, are subject to dishing, a term that refers to low spots in an otherwise relatively flat surface.

If a layer of polysilicon is deposited on the surface of a processed wafer, such as wafer 100, using conventional deposition techniques, and then planarized using conventional CMP processes, dishing tends to remove a significant amount of polysilicon from the top edges of the individual devices. FIGS. 2A and 2B shows cross-sectional diagrams that illustrate the conventional deposition of polysilicon and subsequent planarization using CMP processes.

As shown in FIG. 2A, conventional deposition techniques have been used to form a layer of polysilicon 210 on the top surface 114 of wafer 100. Conventional CMP planarization requires overdepositing of the material to be planarized by 2x-3x the required final thickness. For example, oxide is typically deposited to a thickness of 12K-18K angstroms to obtain a final thickness of 6.5K angstroms.

Current-generation deposition equipment limits the maximum thickness of the deposited polysilicon to approximately 5K angstroms. (Thicker layers of polysilicon produce film stresses that deform the wafer.)

Thus, a final thickness of approximately 2.5K angstroms is the maximum thickness obtainable with current-generation equipment.

Next, as shown in FIG. 2B, polysilicon layer 210 is planarized using chemical-mechanical polishing (CMP) until a thin, substantially-flat layer of polysilicon remains on the surfaces of devices 110. As further shown in FIG. 2B, the CMP process tends to remove more polysilicon at the edges of the top surfaces of devices 110 than at the centers.

This can lead to degraded device performance where the polysilicon has been thinned as shown by arrow A, to an outright open circuit where the polysilicon has been completely removed at the edges as shown by arrow B. Thus, there is a need for a method of forming a thin, planarized layer of polysilicon on the devices which is not subject to polysilicon thinning at the edges of the top surfaces of the devices.

SUMMARY OF THE INVENTION

A method of planarizing a layer of semiconductor material formed on a wafer is disclosed in accordance with a first embodiment of the present invention. The wafer has a top surface, and the top surface has a first region and a second region that lies above the first region. The first region is equal to a lowest part of the top surface. The second region is equal to a highest part of the top surface.

The method includes forming a layer of first material to contact the top surface of the wafer. The layer of first material has a top surface, and the top surface of the layer of first material has a first region and a second region that lies above the first region of the layer of first material. The first region of the layer of first material is equal to a lowest part of the top

surface of the layer of first material. The second region of the layer of first material is equal to a highest part of the top surface of the layer of first material.

The method also includes forming a layer of second material to contact the top surface of the layer of first material. The layer of second material has a top surface, and the top surface of the layer of second material has a first region and a second region that lies above the first region of the layer of second material. The first region of the layer of second material is equal to a lowest part of the top surface of the layer of second material. The second region of the layer of second material is equal to a highest part of the top surface of the layer of second material. The first region of the top surface of the layer of second material lies above the second region of the top surface of the layer of first material.

The method further includes performing a chemical-mechanical polish of the layer of second material and the layer of first material. The chemical-mechanical polish continues until the layer of second material has been substantially all removed from the layer of first material, thereby forming the layer of first material to have a substantially planar top surface. The substantially planar top surface of the layer of first material lies over the first region and the second region of the top surface of the wafer.

A method of planarizing a layer of semiconductor material formed on a wafer is disclosed in accordance with a second embodiment of the present invention. The wafer has a top surface, and the top surface has a first region and a second region that lies above the first region. The first region is equal to a lowest part of the top surface. The second region is equal to a highest part of the top surface.

The method includes conformally forming a layer of first material to contact the top surface of the wafer. The layer of first material has a top surface, and the top surface of the layer of first material has a first region and a second region that lies above the first region of the layer of first material. The first region of the layer of first material is equal to a lowest part of the top surface of the layer of first material. The second region of the layer of first material is equal to a highest part of the top surface of the layer of first material.

The method also includes forming a layer of second material to contact and adhere to the top surface of the layer of first material. The method further includes performing a chemical-mechanical polish of the layer of second material and the layer of first material. The chemical-mechanical polish continues until the layer of second material has been substantially all removed from the layer of first material at which time the layer of first material has a substantially planar top surface. The substantially planar top surface of the layer of first material lies over the second region of the top surface of the wafer.

A better understanding of the features and advantages of the present invention will be obtained by reference to the following detailed description and accompanying drawings that set forth an illustrative embodiment in which the principles of the invention are utilized.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional diagram illustrating a prior-art processed wafer 100 following the etch step that defines the individual devices that make up the circuits on wafer 100.

FIGS. 2A and 2B are cross-sectional diagrams illustrating the conventional deposition of polysilicon and subsequent planarization using CMP processes.

FIGS. 3A-3D are cross-sectional drawings illustrating a method of forming a thin, planarized layer of polysilicon in accordance with the present invention.

DETAILED DESCRIPTION

FIGS. 3A-3D show cross-sectional drawings that illustrate a method of forming a thin, planarized layer of polysilicon in accordance with the present invention. As shown in FIG. 3A, the method utilizes a conventionally processed semiconductor wafer 300 that has a top surface 310. Surface 310, in turn, has a number of substantially-equal lower levels 312 and a number of substantially-equal upper levels 314 that lie above the lower levels 312.

As further shown in FIG. 3A, the method begins by depositing a layer of polysilicon 320 on surface 310. Polysilicon layer 320 is conformally deposited and, as a result, also has a top surface 321 that has a number of substantially-equal lower levels 322 and a number of substantially-equal upper levels 324 that lie above the lower levels 322.

Next, polysilicon layer 320 is conventionally doped. (Alternately, a doped layer of polysilicon can be formed in lieu of separate deposition and doping steps.) Following this, a layer of sacrificial oxide 330 is formed on polysilicon layer 320. Oxide layer 330 is also conformally formed and, like polysilicon layer 320, has a top surface 331 that has a number of

substantially-equal lower levels 332 and a number of substantially-equal upper levels 334 that lie above the lower levels 332.

After this, as shown in FIG. 3B, oxide layer 330 and polysilicon layer 320 are chemically-mechanically polished until oxide layer 330 is substantially, completely removed from the surface of polysilicon layer 320 to form a planarized layer of polysilicon 340. Once planarized polysilicon layer 340 has been formed, as shown in FIG. 3C, a mask 341 is formed and patterned on planarized polysilicon layer 340.

Next, planarized polysilicon layer 340 is etched to form a number of structures, such as local interconnect lines, that are electrically connected to individual devices on wafer 300. (The locations where the structures make electrical contacts with the individual devices of wafer 300 are prepared before polysilicon layer 320 is deposited, and are assumed to be a part of wafer 300.)

Alternately, after the planarization step, one or more additional layers of material, such as materials which lower the resistance of polysilicon, can be formed over layer 340. As shown in FIG. 3D, a layer of material 342 is formed over is formed over planarized polysilicon layer 340. Mask 341 is then formed and patterned on the additional layers of material (e.g., layer 342) which are then etched along with planarized polysilicon layer 340 to form the structures (e.g., local interconnect lines). Either way, once the structures have been formed, the method continues with conventional back-end processing steps.

When the structures are formed, the structures are specified to have a thickness over the upper levels 314 that ranges from a minimum thickness to a maximum thickness. To achieve this result, polysilicon layer 320 is deposited to have a thickness such that lower level 322 is above

upper level 314 by an amount which is at least as great as the minimum specified thickness of the resulting structures.

For example, if the minimum allowable thickness of the resulting structures over upper levels 314 is X (see FIG. 3B), then polysilicon layer 320 must be deposited so that lower level 322 is above upper level 314 by a value that is equal to or greater than the distance X (see FIG. 3A). (If the polishing is timed using experimentally derived values, then polysilicon layer 320 is deposited so that lower level 322 is above upper level 314 by more than the distance X. This allows polysilicon layer 320 to be slightly over etched to insure that oxide layer 330 has been removed while still meeting the minimum requirements for the thickness of the resulting structures.)

In addition, oxide layer 330 is formed to have a thickness such that the combined thickness of polysilicon layer 320 and oxide layer 330 is approximately 2x-3x the required final thickness of the polysilicon layer. (Thicker layers of oxide can be used, but to no apparent advantage.)

Oxide layer 330 and polysilicon layer 320 are chemically-mechanically polished with a slurry that ideally has a selectivity of 1:1 (removes oxide layer 330 at the same rate as polysilicon layer 320). In the present invention, slurries that fall within a range of approximately 0.9-1.1:1 can also be used. This approximate range is a critical range in that slurries that fall well outside of this range produce unacceptable dishing. (Slurries with a selectivity of 1.1:1 are commercially available.)

Although described with respect to polysilicon and oxide, materials other than oxide can alternately be used as a sacrificial material if the material can be removed with a slurry that has a selectivity in the range of 0.9-1.1:1. In addition, the present invention applies to other thin films that

can not be planarized using chemical-mechanical polishing. In this case, the other thin-film is combined with a material that can be removed with a slurry that has a selectivity in the range of 0.9-1.1:1.

It should be understood that various alternatives to the embodiment of the invention described herein may be employed in practicing the invention. Thus, it is intended that the following claims define the scope of the invention and that methods and structures within the scope of these claims and their equivalents be covered thereby.